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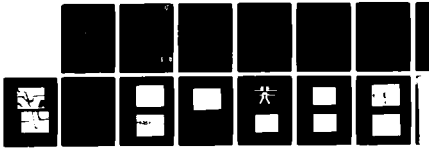

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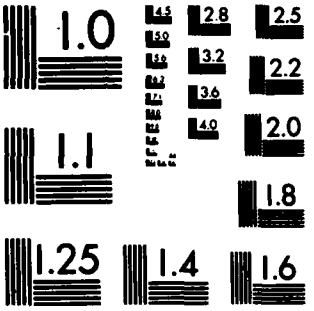

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# Silicon Medium Power MESFET

Contract No. N00014-80-C-0862

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Prepared by: J. Barnard
C. A. Lee
J. Frey

Cornell University
School of Electrical Engineering
Ithaca, NY 14853

Final Progress Report
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## I. Introduction

We have studied the feasibility of using SOS MESFETs in the medium power microwave regime and have fabricated various devices to determine the correlation between expected and measured characteristics.

The conventional silicon-on-sapphire (SOS) medium power MESFET has both a distinct advantage and disadvantage over a GaAs MESFET of similar geometry. The single crystal sapphire substrate is an excellent medium for certain microwave elements, such as microstrip lines. The disadvantage of the conventional SOS MESFET lies in the large source-gate resistance arising from the low mobility of electrons in n-type SOS films. The large source-gate resistance reduces the mutual transconductance ($g_m$) and hence the high frequency figure of merit $f_T$.

## II. Background

### a) Performance of idealized MESFET in saturation region

Transconductance ($g_m$) of the MESFET in the saturation region can be derived as follows:

The depletion width = $d = \frac{2\varepsilon_s V_t}{eN_d}$

with $V_t$ = total voltage = $V_g - V_{bi}$.

The cross-sectional area for current flow is

$$A = (t-d)W$$

Now, if electrons travel at saturated velocity $v_s$, we have a velocity limited current flow through this area,

$$I = N_d e v_s A$$
$$= N_d e v_s (t-d)W$$

Thus, $(g_m) = -\frac{\partial I}{\partial V_t} = \frac{N_d e v_s W}{2} \frac{2\varepsilon_s}{eN_d V_t}$

$$= v_s W \frac{N_d \varepsilon_s e}{2V_t}$$

For example, with $N_d = 10^{17}$ cm$^{-3}$

$v_s = 10^7$ cm/sec

$\varepsilon_s = 13 \times 8.854 \times 10^{-14}$ fcm$^{-1}$

$V_t = 0.6$ ($V_{bi} = -0.6$V and $V_g = 0$V)

$g_m = 124$ mS/mm

For a 1 μm gate length we would expect d to be of the order of .1μ, and

$$C = \frac{A\varepsilon}{d} = \frac{10^{-4} \times .1 \times 13 \times 8.854 \times 10^{-14}}{d} = 1.24 \text{ pF}$$

Thus, $f_T = \frac{g_m}{2\pi C_g} = 16$ GHz

b. Effect of source-gate resistance

The effect of source-gate resistance ($R_{SG}$) is to reduce the intrinsic transconductance, $g_m^i$, to an observed transconductance $g_m^o$.

$$g_m^o = \frac{g_m^i}{1+g_m^i R_{SG}}$$

For the previous example, if we have a 2000Å channel doped to $1 \times 10^{17}$cm$^{-3}$, and effective source to gate spacing of 1 μm and a typical low field mobility in SOS of 600 cm$^2$v$^{-1}$sec$^{-1}$,

$$R_{SG} = \frac{\rho \ell}{A} = \frac{1}{en\mu} \frac{\ell}{A} = 5.2\Omega$$

$g_m^o = 75$ mS, and $f_T = 9.7$ GHz

The deleterious effect of the large source-to-drain resistance resulting from the low mobility for electrons in SOS can be overcome by either reducing the source-drain spacing and/or by increasing the channel doping concentration.

## III. Effect of Increased Channel Doping

### a) Pinch-off voltage

A first order expression for pinchoff voltage is

$$V_p = \frac{qN_d x^2}{2\varepsilon_s}$$

Thus, an increase in $N_d$ can be compensated by reducing epi layer thickness, x, to maintain the required pinch-off voltage.

### b) Breakdown voltage

In bulk Si, the breakdown voltage of a p-n junction decreases with increasing doping on either side according to the empirical result as quoted by Sze for an abrupt junction

$$V_B \approx 60 \left(\frac{E_g}{1.1}\right)^{3/2} \left(\frac{N_B}{10^{16}}\right)^{-3/4} \text{ volts}$$

for $E_g$ the energy band gap in eV and $N_B$ the background doping in $cm^{-3}$. Increasing doping thus reduces breakdown voltage, which might result in reduced maximum permissible output power depending upon device and circuit design.

## IV. Experimental Work

### a) Introduction

The electron saturation velocity in silicon-on-sapphire films has been obtained at Cornell University from pulsed IV measurements. As shown in Fig. 1, this velocity approaches $9 \times 10^6$ cm/sec$^{-1}$ at an electric field of 40 kV cm$^{-1}$ at the top of the layer, where the implanted channel lies. Two-dimensional simulation of silicon MESFETS predict a figure of merit, $f_T$, for the 1μ gate silicon MESFET of 6.2 GHz at $V_{DS}$=5V. Small signal S-parameter measurements performed on devices similar to those fabricated under this contract indicated an $f_T$ of 6.8 GHz. The suitability of SOS MESFETs for medium power amplification in the lower microwave spectrum was subsequently studied both theoretically and experimentally. Noise figure was also measured, and was found to be larger in the SOS MESFETs than in

comparable GaAs MESFETs.

b) Device Fabrication

Our first task was to develop a reliable photolithography process for the lift-off of the aluminum gate using AZ1350J photoresist. Figure 2 shows resist profiles on top of which aluminum would be evaporated for the MESFET gate. The upper SEM photograph shows a metal-to-semiconductor contact length of about 800 nm whereas the opening size is about 1.3 μm. In the lower photograph, the photoresist was dipped into toluene for 2 minutes prior to development. The toluene hardens the resist surface and with a sufficiently long dip in the developer, a pronounced ledge is developed. The optical lithography was performed using a Kasper 10:1 image projector and an optically step-and-repeat generated mask. The metal lifted off more cleanly from the toluene-treated resist but the gate length in the toluene-soaked resist process was larger than in the untreated resist process.

The next step in the process was to pattern the aluminum gates and to sinter the wafer in forming gas ($N_2$+$H_2$) for seven minutes at 425°C. A SEM photograph of the gate structure after a sinter at a higher temperature is shown in Figure 3. The aluminum source was slightly offset to the right of the picture, so giving a small aluminum wall, visible as a bright line on the left hand side of the gate. A more interesting phenomenon can be seen in the upper photograph. Silicon is soluble in aluminum up to about 3% mole fraction and silicon close to the gate pad has here diffused into the large gate pad (100x100 $\mu m^2$), which acts as a sink for silicon atoms. The void formed in the silicon mesa where the aluminum from the gate first meets the silicon increases in size with an increase in sintering temperature. At 425°C for 7 minutes there is no noticable void formation.

The etching of the mesa was performed using the well-known anisotropic hydrazine etchant. This etchant is stopped even by a thin (~10 nm) oxide film on

the silicon and at 80°C etches (100) silicon at about 400 nm/minute. The anisotropic etching which attacks (100) faces about 20 times faster than (111) type faces leaves a mesa with sloping (111) type walls which allow for good metal edge coverage.

On the basis of experience gained during a substantial amount of work on small-signal SOS MESFETs under a previous Navy contract, N00173-78-C-0435, it was decided to use nominally intrinsic SOS films, rather than n-doped films, as the starting material. Both the channel and the source-drain regions were then doped by ion implantation. A further improvement involved using ion milling to open the source-drain windows in the 200 nm oxide. The milling was continued a little into the SOS film so that the source and drain region parameters could be seen for later alignment of both the mesa and the metallization to the source-drain n+ regions.

Many different processes were tried until the optimum planar SOS MESFET process was established. This process is shown in Figure 4. In this process the nominally undoped SOS wafer was covered with 170 nm of spin-on oxide, and then placed in a wet oxidation furnace at 900°C for 30 minutes to densify and thicken the oxide layer to 200 nm. Since the low-field mobility of electrons on the silicon layer decreases rapidly from the surface towards the Si/sapphire interface, it is imperative to lose as little silicon from the SOS surface as possible - hence the use of spin-on oxide film as opposed to the use of a long wet oxidation time to grow 200 nm of oxide. The temperature must be kept below 930°C to prevent excessive propagation of defect and diffusion of aluminum from the sapphire into the silicon layer. The diffusion time must similarly be minimized.

The source-drain regions are patterned in AZ1350J resist by 10:1 image reduction-projection photolithography. The oxide in the opened windows is removed by precise ion milling using a 500V argon ion beam at a density of 50 mA $cm^{-2}$. A thin 20 nm oxide is then grown in the source-drain windows to

reduce the damage caused by the ion beam, and to keep the source and drain regions clean during the anneal that follows the phosphorous implant. The n+ regions were formed by a 60 keV phosphorous implant at $3x10^{15}cm^{-2}$. The anneal took place in nitrogen at 850°C for 30 minutes. Following the anneal, all the oxide was stripped from the wafer by etching the SOS wafer for five minutes in buffered HF.

A thin (~12 nm) oxide was grown on the wafer by dipping it into hot nitric acid. After this the channel was formed by implanting $1.5x10^{12}$ $cm^{-2}$ phosphorous atoms into the SOS film at 120 keV. A 750°C anneal in nitrogen followed for 30 minutes. This low anneal temperature was necessary to prevent diffusion of the phosphorous, but did achieve 85% activation of the phosphorous.

The unwanted silicon was etched away using hydrazine anistropic etching to leave the structure shown in Figure 5. The thin oxide was then removed by an HF etch. The gate is not recessed in this structure.

The final step in the process involved the lift-off of 250 nm of aluminum to form the source, drain and gate metallizations. The aluminum on the channel formed the Schottky barrier gate while the aluminum on the n+ source and drain regions formed ohmic contacts. The electrical characteristics of the transistors were measured after the wafer was sintered in hydrogen at 425°C for seven minutes. The lower photograph in Figure 6 shows the final test SOS MESFET with a total gate width of 200 μm. This structure was used in our experiments on medium power SOS MESFETs, where we consider "medium power" MESFETs to cover the spectrum of gate widths from 100 μm to 1mm. Also in the test structure was a resistor and a Schottky diode, which were used to determine differences in electrical characteristics between SOS films and bulk silicon.

c) Electrical test results

The DC drain characteristics for the planar process FET is shown in Figure 7. The measured transconductance ($g_m$) of the MESFET was 23 mS per mm. Using Pucel's formula for a one-dimensional device, $C_{gs}$ was estimated to be .8 pf/mm leading to an estimated $f_T$ = 4.86 Hz.

An improved SOS MESFET with a 80 keV channel implant at $2x10^{12}cm^{-2}$ of phosphorous is shown in Figure 8. The transconductance is 40 mS per mm of gate width and device characteristics are stable out to $V_{DS}$=11V. An SOS MESFET with a one mm gate width can pass about 45 mA at 11V across the drain and source, representing a power-handling capability of about 0.045x11=.5W/mm with a very low pinch-off voltage of -2.0 volts. These medium-power SOS MESFETs can be used to drive 50 Ω lines from high speed SSI where a low pinch-off voltage is necessary. For unity gain, a 20 mS transconductance is called for in a 50Ω system and this of course can be realized using a 500 μm wide gate SOS MESFET.

Additional SOS MESFET processes were developed to check, first, the use of a platinum gate, and second, the scaling of SOS MESFET gate width. In the first case, Figure 9 (top) shows the Pt-gate SOS MESFET drain characteristics with their particularly low knee voltage. The Pt-Si Schottky barrier is of very good quality, and the metallurgical junction is formed below the original SOS surface close to the formation of the Pt-Si silicide. The lower drain characteristics in Figure 9 are for those of a SOS MESFET with a gate width of 1.6 mm and a transconductance at $V_g$=0, $V_{DS}$=10V of about 50 mS. This $g_m$ is slightly degraded from that expected from an extrapolation of the drain characteristics for a 200 μm wide gate device. This discrepancy results from heating of the device due to dissipation of power ranging from 0 mW up to a peak of 800 mW. Thus, we have demonstrated that a medium-power-i.e., one with a power output between 0.1 and 1.0 W/mm gate width-SOS MESFET for 50Ω line driving is realizable. However, the gate will probably have to be in excess of 500 μm wide to achieve the highest of these "medium" power levels.

To get larger currents flowing in the MESFET, a larger dose implant is called for. This has a number of effects. Firstly, the pinch-off voltage is increased. This can be offset by making a shallower implant as mentioned earlier in this report. The figure-of-merit $f_T$ should remain more-or-less constant as both the transconductance and the gate capacitance are increased together. However, in this trade-off in which the gate capacitance is increased, the parasitic capacitance

associated with external circuitry becomes of lesser relative importance and so, although the $f_T$ of the device remains approximately constant, the frequency response of the circuit should increase with increased channel doping. The Schottky gate breakdown voltage unfortunately decreases with increasing channel doping. Several experiments were performed to determine the difference between the breakdown voltage of Schottky barriers on bulk silicon and on SOS films. It was found, in fact, that the breakdown voltage of Schottky barrier gates on SOS films was consistently about 33% higher than for similar barriers on bulk silicon. To firstorder, this phenomenon may be due to the fact that the defect density in SOS films is generally larger than in silicon. This density results in faster carrier cooling in the SOS film at a given field than in bulk silicon, hence the larger electric field needed for avalanching in SOS. In other words, at a given field electrons retain less energy in SOS than in bulk Si; higher fields are necessary to accelerate electrons to ionization-producing energies in SOS than in bulk Si. This larger breakdown voltage will allow the channel of medium power MESFETs to be doped more heavily to reduce the parasitic source-gate resistance, which has such deleterious effects on the observed $g_m$ relative to the intrinsic device $g_m$.

An experiment was performed to determine the suitability of directly writing the Al gate pattern in PMMA and to lift-off submicron gate structures in the resist. Figure 10 shows SEM photographs of the outcome of the experiment in which with very little optimization a 400 nm long uniform gate was produced. Direct writing electron beam lithography with its very sensitive automatic alignment capability should allow for very short source-gate spacings, so further reducing the source-gate parasitic resistance.

## V. Conclusions

We have developed a SOS MESFET process which has produced devices with transconductances up to 40 mS $mm^{-1}$ of gate width. We have found the Pt-gate to have advantages with regard to low knee voltage. A large SOS MESFET, with a 1.6 mm wide gate, exhibited a $g_m$ of about 50 mS and a power handling capability at 10V

on the drain of 0.5 W $mm^{-1}$ gate width. The pinch-off voltage was about -3.0V allowing a similar device with a shorter gate width to be used as a 50Ω line driving transistor on the periphery of an integrated circuit. We found that the SOS MESFET channel can be doped more heavily for a given gate-drain breakdown voltage than a similar device fabricated in bulk silicon. Finally, the capability of the Cambridge EBMF-2/150 electron beam microfabrication machine to directly pattern PMMA on SOS films and to subsequently pattern a 400 nm aluminum gate by lift-off was demonstrated.

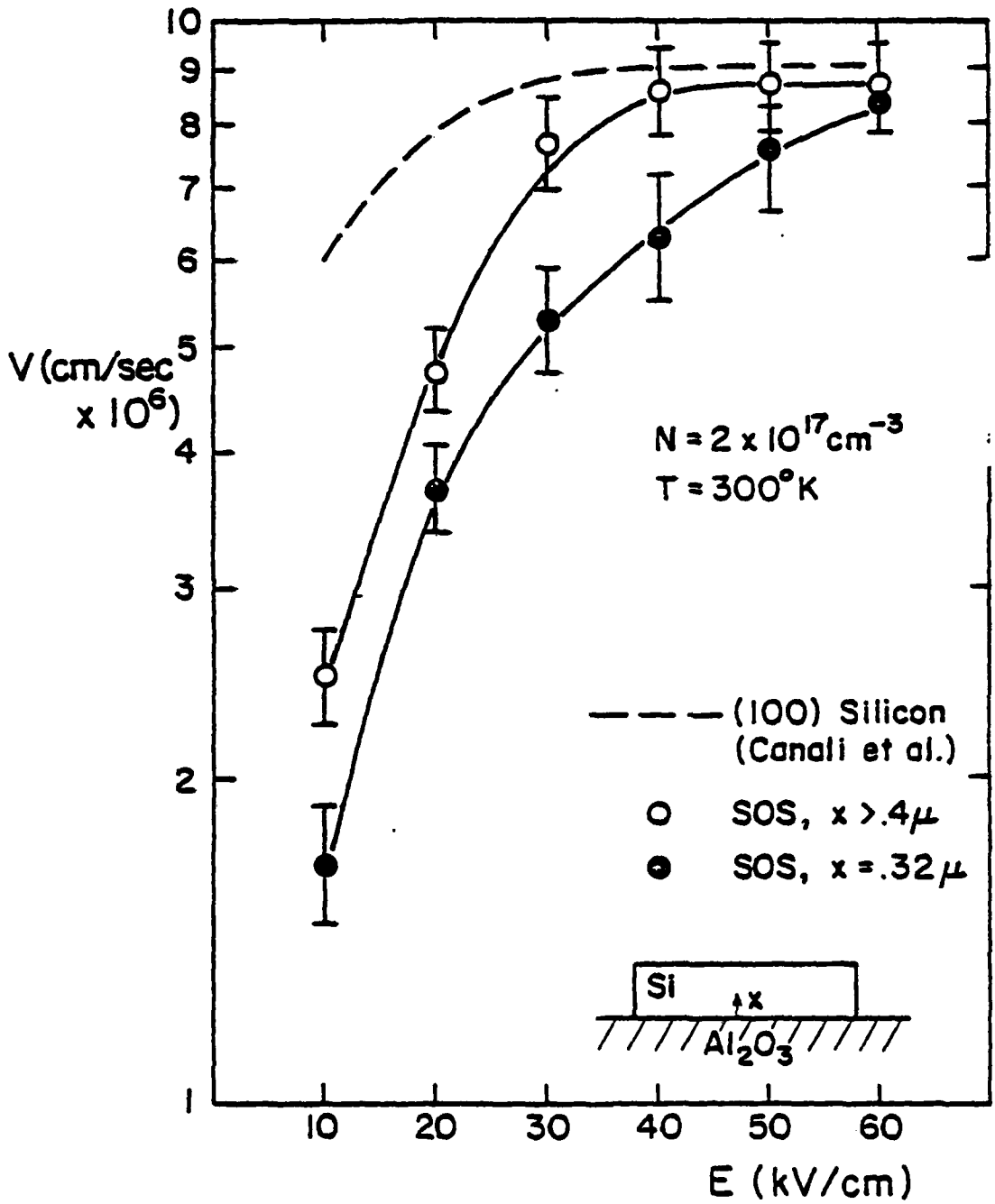
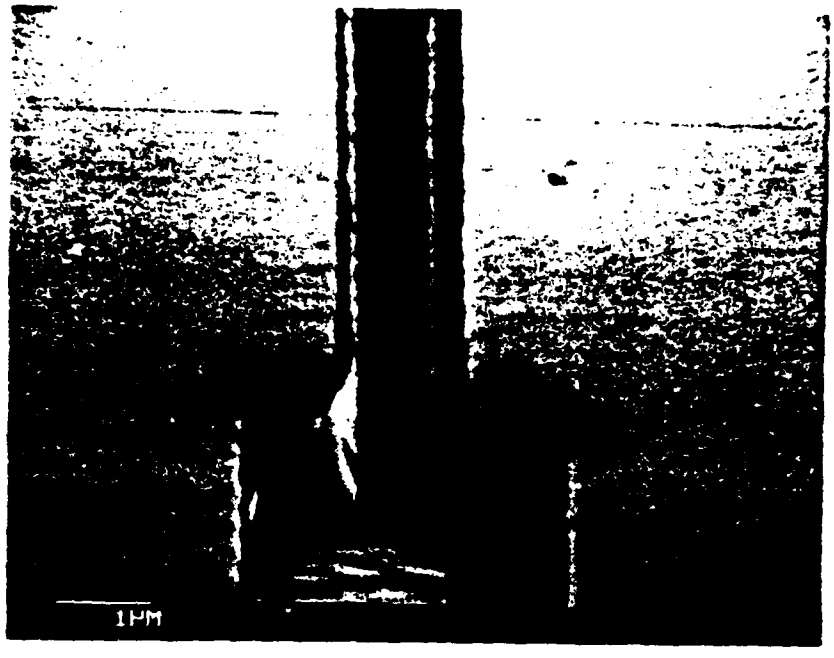
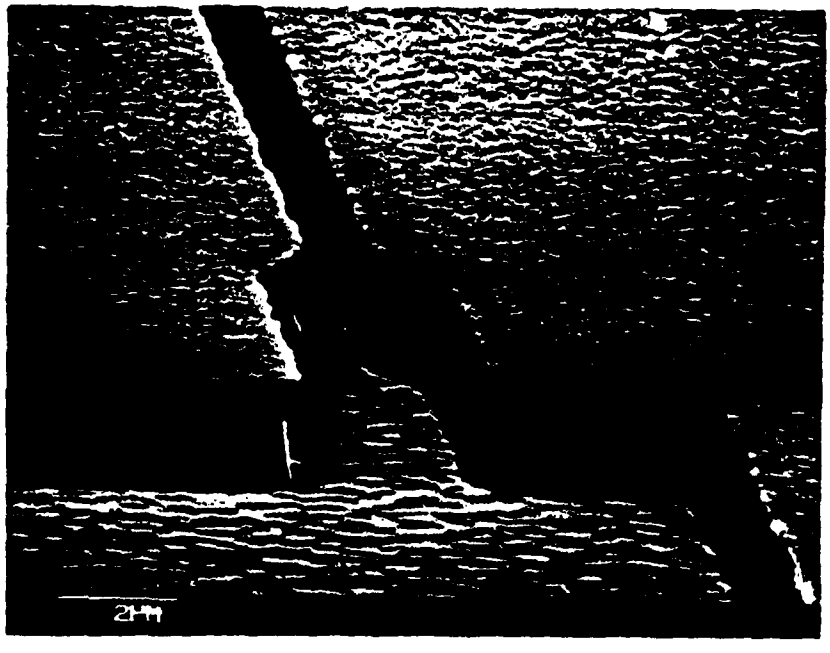



FIGURE 1: ELECTRON SATURATION VELOCITY IN N-TYPE SOS VERSUS ELECTRIC FIELD.

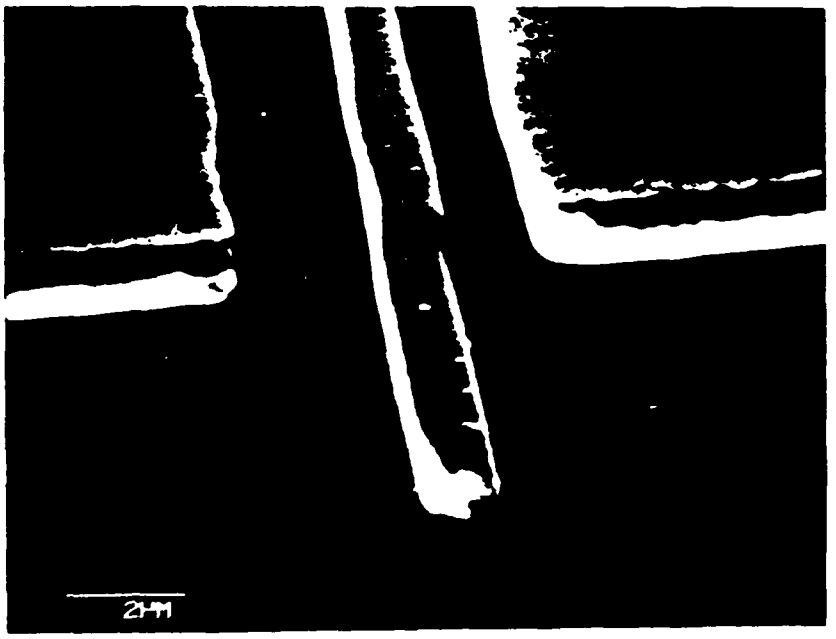
FIGURE 2




DEVELOPED GATE PATTERN IN AZ1350J




AS ABOVE BUT WITH A 2 MINUTE DIP IN TOLUENE PRIOR TO DEVELOPMENT.

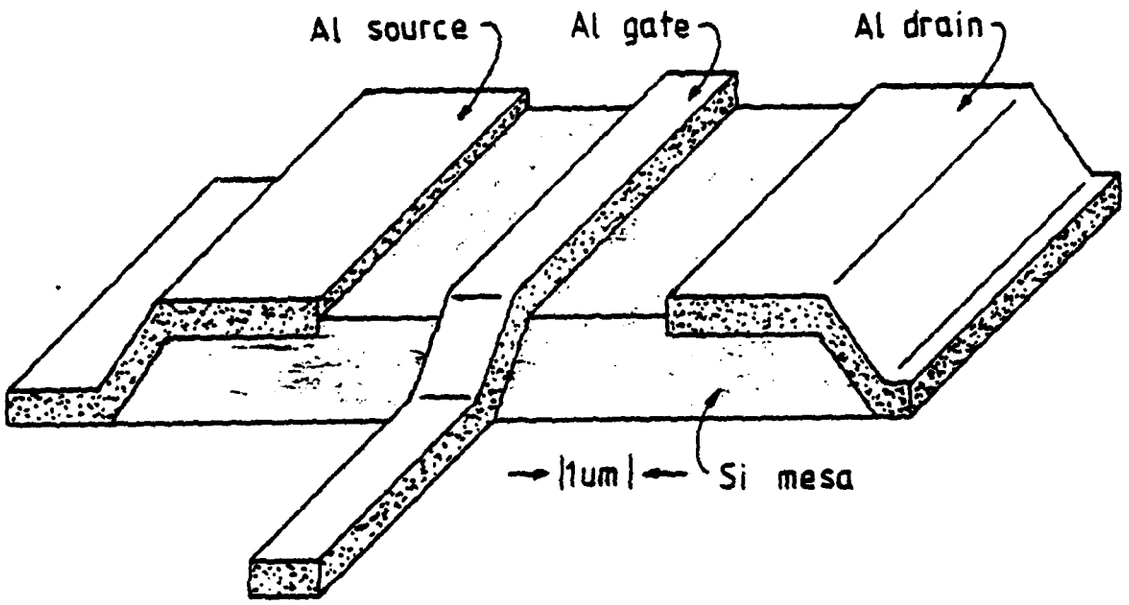

DIFFUSION OF SILICON INTO ALUMINUM.

FIGURE 3

FIGURE 4

## Planar SOS MESFET

- source and drain DIFFUSION or high dose IMPLANT
- MESA ion milled in argon at 500V 500nm
- channel implant 1,5E12cm$^{-3}$ phosphorus at 120 to 160KeV
- METALLISATION 250nm Al lift off



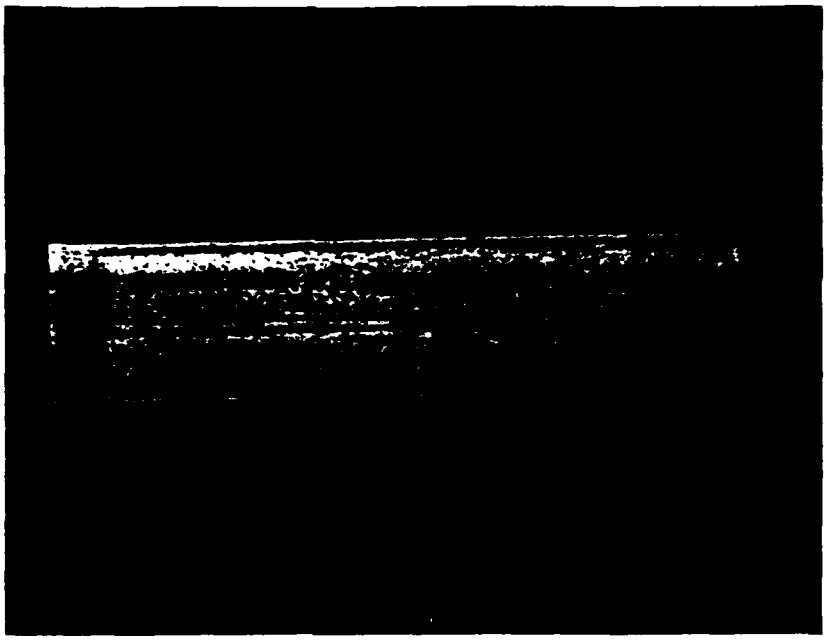


Figure 5: Si Mesa with SD pattern

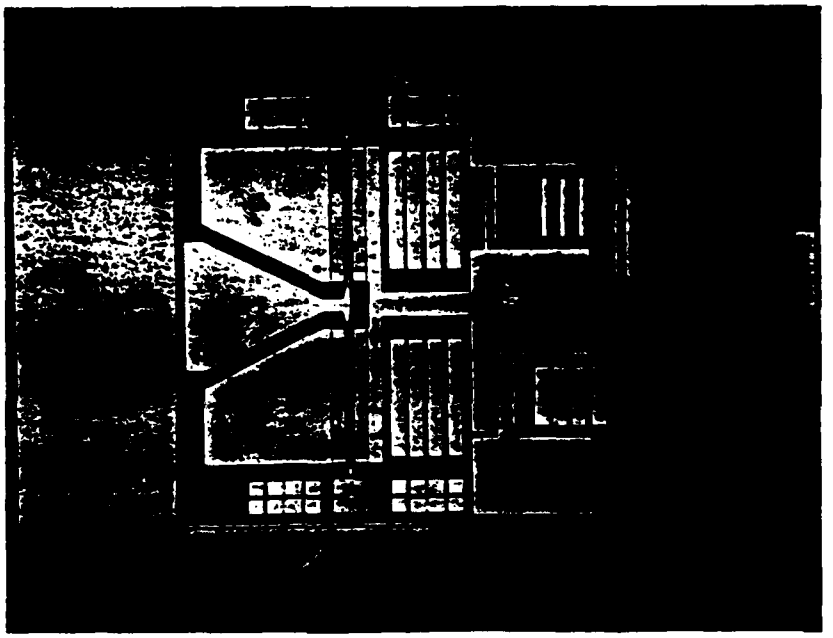
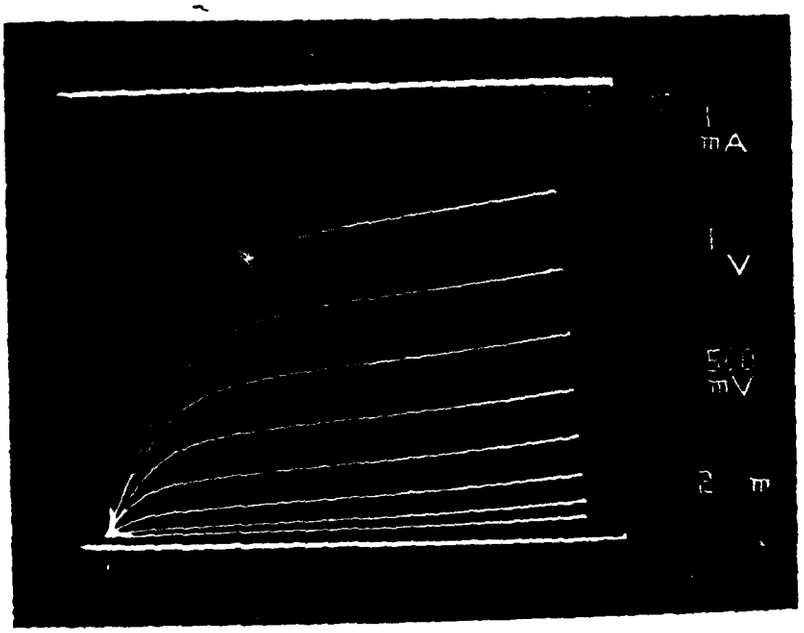


Figure 6: Final SOS MESFET




D.C. DRAIN CHARACTERISTICS FOR PLANAR-PROCESS-FET

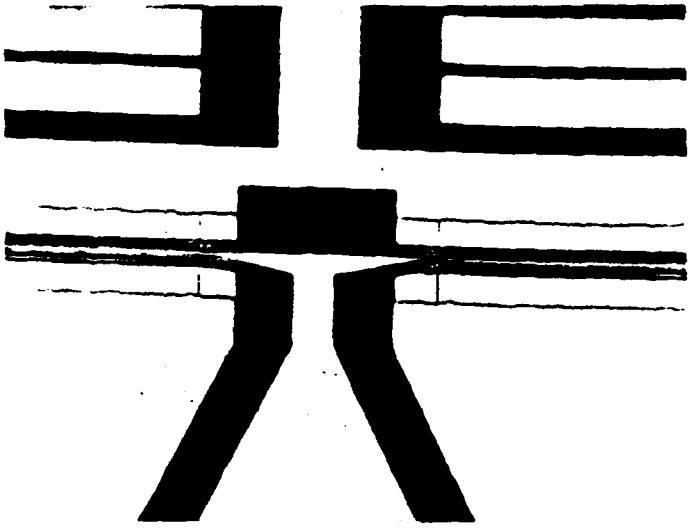
* $G_M$ = 230 MS/CM AT $V_G$ = 0V, $V_{DS}$ = 5V.

* PINCH OFF VOLTAGE = - 3.8V.

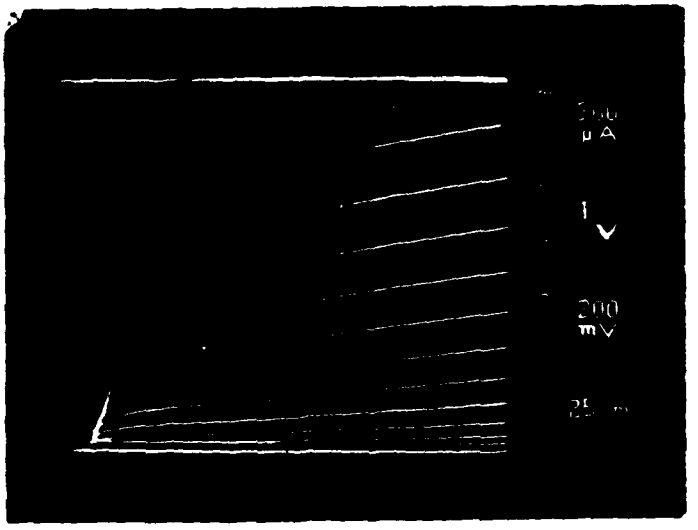
* $F_T$ PREDICTED = 4.8 GHz.

FIGURE 7

FIGURE 8

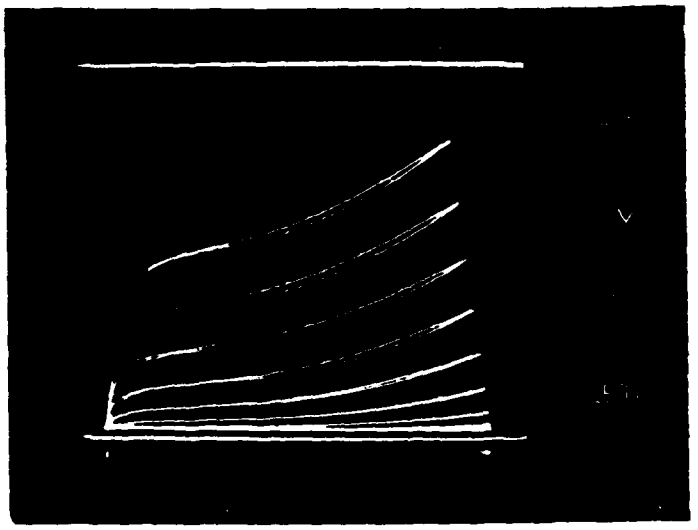


Short channel SOS MESFET with one micron gate length.

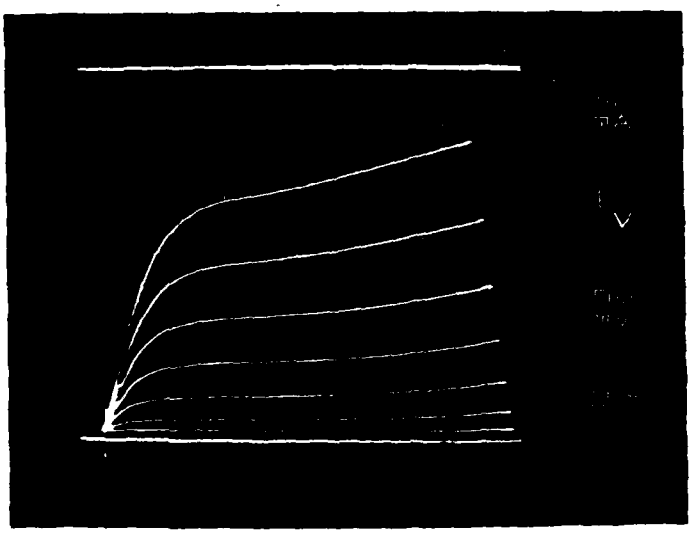



Characteristics of above SOS MESFET exhibiting a transconductance of 40mS per mm gate width.

FIGURE 9

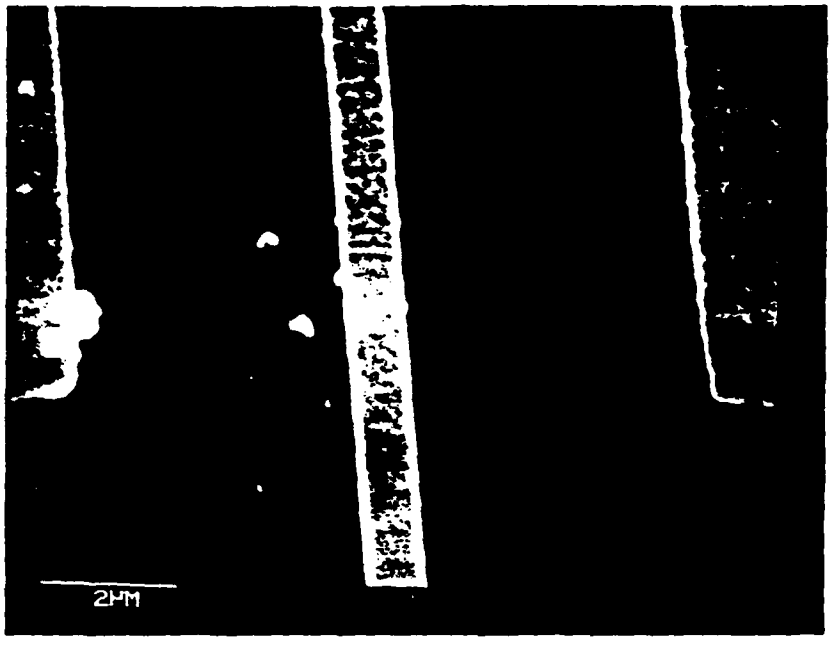


Pt gate Lg = 1μm Wg = 40μm LSD = 3μm

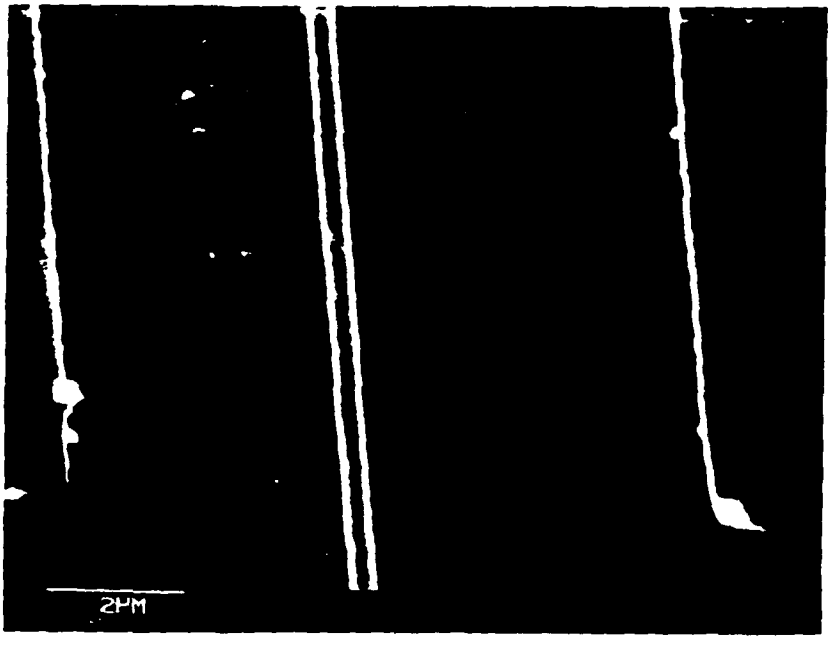


Al gate Lg = 1.2μm Wg = 1.6mm LSD = 3μm

FIGURE 10




Quality of 1um Al gate by lift off using PMMA resist.




Quality of 400nm Al gate by lift off using PMMA resist.